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EXAMINER	
FRANKLIN, RICHARD B	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/813,628	KNOWLES, SIMON	
	Examiner	Art Unit	
	RICHARD FRANKLIN	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 April 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1 - 29 are pending.

Response to Arguments

2. Applicant's arguments filed 14 April 2009 have been fully considered but they are not persuasive.

Applicant argues that the relied upon reference, US Patent No. 6,725,357 (Cousin), does not teach that the decode unit detects if the instruction packet defines at least two control instructions. However, the Examiner respectfully disagrees.

Applicant has defined **"control instructions"** to include **"instructions dedicated to program flow, and branch and address generation; but not data processing"** (Current Application Publication No. 2005/0223193; Paragraph [0026]). Applicant also defines **"data processing instructions"** as **"instructions for logical operations, or arithmetic operations"** (Current Application Publication No. 2005/0223193; Paragraph [0026]).

Applicant's arguments seem to indicate that Applicant has interpreted the "control instructions" of the claimed invention to only be the instructions formatted for the general unit of Cousin. However, this is not the interpretation taken by the Examiner. The Examiner has interpreted both the instructions formatted for the general unit and the instructions formatted for the address units to be the "control instructions." The address units of Cousin are defined as executing instructions for memory accesses to a data memory (Cousin; Col 5 Lines 18 – 20). The general unit of Cousin is also defined

as executing branch instructions (Cousin; Col 5 Lines 23 – 26). These definitions are consistent with Applicants definition of "control instructions," shown above. Therefore, the address unit instructions and general unit instructions are both "control instructions."

Cousin shows that instructions included within instruction packets are decoded by decode unit 8 into either data processing instructions which are sent to data units DU0 and DU1 or control instructions which are sent to address units AU0 and AU1 or general unit GU (Cousin; Col 4 Line 4 – Col 5 Line 13). Cousin also teaches that in VLIW mode, a plurality of each data processing instructions and control instructions are simultaneously detected and queued (Cousin; Col 4 Line 66 – Col 5 Line 13).

Therefore, using the Examiner's interpretation of "control instructions," it can be seen that Cousin discloses that the decode unit detects if the instruction packet defines at least two control instructions.

Continued Examination Under 37 CFR 1.114

3. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 14 April 2009 has been entered.

4. All claims are drawn to the same invention claimed in the application prior to the entry of the submission under 37 CFR 1.114 and could have been finally rejected on the

grounds and art of record in the next Office action if they had been entered in the application prior to entry under 37 CFR 1.114. Accordingly, **THIS ACTION IS MADE FINAL** even though it is a first action after the filing of a request for continued examination and the submission under 37 CFR 1.114. See MPEP § 706.07(b). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1 – 3, 7 – 10, 12, 14, 16 – 19, 21, 23, 25 – 26, and 29 rejected under 35 U.S.C. 102(e) as being anticipated by US Patent No. 6,725,357 (hereinafter Cousin).

As per independent claim 1, Cousin teaches a computer processor, the processor comprising: (a) a decode unit for decoding a stream of instruction packets from a memory (Cousin; Figure 1, element 8 receiving instructions from element 2), each instruction packet comprising a plurality of instructions (Cousin; Col. 3, Lines 28 – 31; "... a number.., of instructions..."); (b) a first processing channel (Cousin; Figure 1, elements EXU3 – EXU5; Examiner's note: it is clear by elements D-IDQ and A-IDQ that there exists two separate channels.) comprising a plurality of functional units (Cousin, Figure 3, elements 143, 114) and operable to perform control processing operations (Cousin; Col. 5, Lines 17 – 26, "branch circuitry..." etc.); (c) a second processing channel (Cousin; Figure 1, elements EXU1 – EXU2; Examiner's note: it is clear by elements D-IDQ and A-IDQ that there exists two separate channels) comprising a plurality of functional units (Cousin; Figure 3, elements DU0-1) and operable to perform data processing operations (Cousin; Col. 5, Lines 17 – 18); wherein the decode unit is operable to receive an instruction packet (Cousin; Col. 3, Lines 28 – 31) and to detect (Cousin; Col. 4, Lines 15 – 19) if the instruction packet defines (i) a plurality of control instructions (Cousin; Col. 4, Lines 19 – 22 "... address units...general unit...") or (ii) a plurality of instructions one or more of which is a data processing instruction (Cousin; Col. 4, Lines 19 – 22 "...data units..."), and wherein when the decode unit detects that the instruction packet comprises a plurality of control instructions said control instructions are supplied to the first processing channel for execution in program

order(Cousin; Col. 4, Lines 15 – 19 and Col. 7, Lines 3 – 15; Examiner's note: Cousin discloses a macro instruction being decoded into multiple micro operations and being routed to the appropriate channels (beginning with queues D-IDQ, A-IDQ). It is clear from all of the cites in this paragraph that Cousin distinguishes between control instructions (address and branch) and data instructions (essentially integer operations) as illustrated by the two separate data paths shown in Figure 3. Cousin also teaches that program order is maintained).

As per claim 2, Cousin teaches the decode unit [being] operable to detect an instruction packet comprising three control instructions and control the control process to execute each of the three control instructions in the order in which they appear in the instruction packet (Cousin; Col. 4, Lines 57 – 60; Examiner's note: Since the instruction in the cite contains eight instructions and up to eight can be control instructions, it is clear that Cousin discloses the ability to decode three control instructions.).

As per claim 3, Cousin teaches the decode unit [being] operable to detect an instruction packet containing a plurality of control instructions of equal length (Cousin; Figure 2; Examiner's note: Figure 2 shows macroinstructions containing microinstructions of equal length.).

As per claim 7, Cousin teaches the decode unit [being] operable to detect when there is at least one data processing instruction in the instruction packet and, in

response thereto, to cause relevant data to be supplied to the data processing channel (Cousin; Col. 4, Lines 15 – 19).

As per claim 8, Cousin teaches the decode unit being operable to detect that the instruction packet comprises at least one data processing instruction and a further instruction selected from one or more of." a memory access instruction; a control instruction; and a data processing instruction (Cousin; Col. 4, Lines 15 – 22; Examiner's note: It is clear from Figure 3, that the "address unit" and "general unit" are designed to handle control instructions and memory accesses.).

As per claim 9, Cousin teaches at least one data processing instruction and said further instruction are executed simultaneously (Cousin; Col. 3, Lines 10 – 13).

As per claim 10, Cousin teaches the second processing channel is dedicated to the performance of data processing operations (Cousin; Col. 3, Lines 37 – 39) and data processing instructions are provided in assembly language (Cousin; Col. 3, Lines 15 – 18; Examiner's note: It would have been common at the time of invention to require the macro-instructions to be written in assembly code as was a common standard at the time of invention.).

As per claim 12, Cousin teaches the first processing channel [comprising] units selected from one or more of." a control register file (Cousin; Figure 3, element 16; Col.

5, Lines 40 – 44); a control execution unit (Cousin; Figure 3, element 143); a branch execution unit (Cousin; Figure 3, element 114) and a load/store unit (Cousin; Figure 3, element 150; Col. 3, Line 60 to Col. 4, Line 4).

As per claim 14, Cousin teaches the second processing channel [comprising] a data execution path including a fixed data execution unit (Cousin; Figure 3, element 133).

As per claim 16, Cousin teaches the fixed data execution unit [operating] according to single instruction multiple data principles (Cousin; Figure 3, elements 133; Examiner's note: Cousin discloses two execution units in parallel capable of acting in an SIMD manner.).

As per claim 17, Cousin teaches the data processing channel [comprising] one or more of a data register file (Cousin; Figure 3, element 12) and a load/store unit (Cousin; Figure 3, element 150; Col. 3, Line 60 to Col. 4, Line 4).

As per claim 18, Cousin teaches a single load/store unit [being] accessed by both the control processing channel and the data processing channel through respective ports (Cousin; Figure 3, element 150; Col. 3, Line 60 to Col. 4, Line 4).

As per claim 19, Cousin teaches the decode unit [being] operable to detect an instruction packet comprising at least one data processing instruction (Cousin; Col. 4, Lines 15 – 22), wherein the bit length of the at least one data processing instruction is between 30 and 38 bits (Cousin; Figure 2, GP32 instruction and VLIW instruction).

As per claim 21, Cousin teaches the decode unit [being] operable to detect an instruction packet comprising a data processing operation and a memory access instruction (Cousin; Col. 4, Lines 15 – 22; Examiner's note: It is clear from Figure 3, that the "address unit" and "general unit" are designed to handle control instructions and memory accesses and "data unit" able to handle data processing instructions).

As per claim 23, Cousin teaches the decode unit [being] operable to detect an instruction packet comprising a data processing instruction and a control processing instruction (Cousin; Col. 4, Lines 15 – 22; Examiner's note: It is clear from Figure 3, that the "address unit" and "general unit" are designed to handle control instructions and memory accesses and "data unit" able to handle data processing instructions).

As per claim 25, Cousin teaches wherein the decode unit is operable to detect a data processing instruction in assembly language (Computers all operate on the assembly language level).

As per independent claim 26, independent claim 26 is rejected as being the method performed by the apparatus in independent claim 1.

As per independent claim 29, Cousin teaches a computer readable medium bearing an instruction set for a computer including a first class of instruction packets each comprising a plurality of control instructions for execution sequentially (Cousin; Col. 4, Lines 56 – 60; Examiner's note: Cousin allows for an instruction packet containing only control words.) and a second class of instruction packets each comprising at least a data processing instruction and a further instruction for execution contemporaneously (Cousin; Col. 4, Lines 56 – 60; Examiner's note: In the same cite, Cousin allows for differing types of operations "... in each p slot 0 and p slot 1 of either the data units DUO and DU1 or the address units AU0 and AU1/general unit GU."), said further instruction being selected from one or more of." a memory access instruction; a control instruction; and a data processing instruction (Cousin; Col. 4, Lines 15 – 22 and Col. 7, Lines 3 – 15; Examiner's note: It is clear from Figure 3, that the "address unit" and "general unit" are designed to handle control instructions and memory accesses and "data unit" able to handle data processing instructions. With regard to Col. 4, Lines 56 – 60, since an instruction packet can send instructions to each of these units simultaneously, it stands that there can be all three operations in one packet. Cousin also teaches that program order is maintained).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 4 – 5, 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,725,357 (hereinafter Cousin) in view of US Patent No. 6,880,150 (hereinafter Takayama).

As per claim 4, Cousin teaches the limitations as stated in claim 3.

Cousin does not disclose detecting within an instruction packet a control instruction of a bit length between 18 and 24 bits.

Takayama teaches detecting within an instruction packet a control instruction of a bit length between 18 and 24 bits (Takayama; Col. 13, Lines 29 – 33).

The advantage of using control instructions that are between 18 and 24 bits in length (21 bits as disclosed by Takayama) would have been to allow control instructions to be executed even when other operations are performed in units of an integer number of bytes (Takayama; Col. 2, Lines 9 – 13). This advantage is desirable, as it would have increased execution speed of control instructions and thus the entire system. This advantage would have motivated one of ordinary skill in the art to modify the instruction set to accommodate a 21-bit control instruction as disclosed by Takayama within the processor disclosed by Cousin.

As per claim 5, Cousin and Takayama disclose the limitations as stated in claim 4.

Takayama further teaches detecting within an instruction packet a plurality of control instructions each having a bit length of 21 bits (Takayama; Col. 13, Lines 29 – 33).

The advantage of using control instructions that are 21-bits in length would have been to allow control instructions to be executed even when other operations are performed in units of an integer number of bytes (Takayama; Col. 2, Lines 9 – 13). This advantage is desirable, as it would have increased execution speed of control instructions and thus the entire system. This advantage would have motivated one of ordinary skill in the art to modify the instruction set to accommodate a 21-bit control instruction as disclosed by Takayama within the processor disclosed by Cousin.

As per claim 11, Cousin teaches the limitations as stated in independent claim 1.

Cousin does not disclose control processing operations [being] performed on operands up to a first predetermined bit width and the data processing operations [being] performed on data up to a second pre-determined bit width, the second pre-determined bit width being larger than the first pre-determined bit width.

Takayama teaches control processing operations [being] performed on operands, up to a first predetermined bit width and the data processing operations [being] performed on data up to a second pre-determined bit width, the second pre-

determined bit width being larger than the first pre-determined bit width (Takayama; Col. 13, Lines 29 – 33; Examiner's note: Use of 21-bit and 42-bit instructions.).

The advantage of using control instructions that are 21-bits in length would have been to allow control instructions to be executed even when other operations are performed in units of an integer number of bytes (Takayama; Col. 2, Lines 9 – 13). This advantage is desirable, as it would have increased execution speed of control instructions and thus the entire system. This advantage would have motivated one of ordinary skill in the art to modify the instruction set to accommodate a 21-bit control instruction as disclosed by Takayama within the processor disclosed by Cousin.

7. Claims 6, 22 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,725,357 (hereinafter Cousin).

As per claim 6, Cousin teaches the limitations as stated in independent claim 1.

Cousin does not explicitly disclose the decode unit [being] operable to receive and decode instruction packets of a bit length of 64 bits.

However, it would have been obvious to one of ordinary skill in the art at the time of invention that the length of the instruction packet could be modified to allow for a more standard length depending on which instruction set architecture is to be used, such as the 64-bit IA-64 ISA. Furthermore, Cousin does not limit the size of a packet as the only criterion for decoding is that the instruction be divisible by two or four. Thus it is clear that the size of an instruction is not the main focal point stressed by Cousin and

therefore could be tailored to fit a certain instruction set more suited to a particular application.

As per claim 22, Cousin teaches the limitations as stated in independent claim 1.

Cousin does not explicitly disclose the bit length of said memory access instruction [being] 28 bits.

However, it would have been obvious to one of ordinary skill in the art at the time of invention that the bit lengths of instructions disclosed in Cousin are of little significance and the primary concern set forth by Cousin is merely the alignment of instructions within the packet (Figure 2). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to utilize a smaller instruction size than 32 bits in the invention disclosed by Cousin with the goals of either saving space or adapting the invention to a customized standard. Furthermore, it would have been obvious to one of ordinary skill in the art at the time of invention that the size of an individual word is of no consequence given the words are still aligned properly as disclosed by Cousin.

As per claim 24, Cousin teaches the limitations as stated in independent claim 1.

Cousin does not explicitly disclose the decode unit [being] operable to detect a control processing instruction in C code or variant thereof.

However, it would have been obvious to one of ordinary skill in the art at the time of invention to enable a processor to support higher level languages, such as C, as the

languages are easier to develop code in and are more commonly used to develop code in. Therefore, it would have been obvious to allow a user to utilize an easier language such as C to code control instructions.

8. Claims 13 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,725,357 (hereinafter Cousin) in view of US Patent No. 5,956,518 (hereinafter DeHon).

As per claim 13, Cousin teaches the limitations as stated in independent claim 1.

Cousin does not disclose the second processing channel [comprising] a data execution path including a configurable data execution unit.

DeHon does disclose a data execution path including a configurable data execution unit (DeHon; Col. 5, Lines 23 – 26).

The advantage of using a configurable data execution unit in place of a fixed execution unit would have been to allow greater flexibility for processing ability, as would have been known to one of ordinary skill in the art at the time of invention (DeHon; Col. 1, Lines 41 – 47). The idea of utilizing a programmable chip, such as an FPGA, would have been very common at the time of invention and furthermore, the benefits of reprogrammable processing to implement a variety of application specific functions would have been common at the time of invention. The advantage of using a configurable execution unit would have been to allow for a seemingly infinite amount of processing capability with a relatively low amount of chip space needed, as the programmable units could be reprogrammed if necessary. This advantage would have

motivated one of ordinary skill in the art to utilize the programmable datapath ideas disclosed by DeHon in the invention disclosed by Cousin for the purpose of providing a more robust processor.

As per claim 15, Cousin and DeHon disclose the limitations as stated in claim 14.

Cousin does not disclose the configurable data execution unit [operating] according to single instruction multiple data principles.

DeHon does disclose the configurable data execution unit [operating] according to single instruction multiple data principles (DeHon; Col. 5, Lines 23 – 26).

The advantage of using a SIMD architecture as disclosed by DeHon would have been to enable the processor disclosed by Cousin to more efficiently handle large quantities of data in parallel. Given the parallel nature of the processor disclosed by Cousin, it would have been obvious to one of ordinary skill in the art at the time of invention that an SIMD architecture would have further increased the data processing capabilities of a data processing execution unit. Furthermore, with the increasing use of DSP processors, a move to an SIMD architecture in the data execution channel would have enable one to utilize the processor disclosed by Cousin in a competitive nature with other DSP processors utilizing an SIMD architecture. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to use an SIMD architecture disclosed by DeHon within the data processing channel disclosed by Cousin for the purpose of increasing data throughput in an environment operating on large quantities of data.

9. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,725,357 (hereinafter Cousin) in view of "Variable Length Instruction Compression for Area Minimization", Piia Simonen, Ilkka Saastamoinen, Jari Nurmi, 2003, IEEE (hereinafter Simonen).

As per claim 20, Cousin teaches the limitations as stated in claim 19.

Cousin further disclose the decode unit [being] operable to detect an instruction packet comprising at least one data processing instruction.

Cousin does not disclose a bit length of the at least one data processing instruction is 34 bits.

Simonen teaches a bit length of the at least one data processing instruction is 34 bits (Simonen; Section 3.1 ("Control Bits"), Lines 3 – 4.).

The advantage of utilizing a 34-bit data processing instruction would have been to reduce the amount of space needed to implement certain data processing instructions (Simonen; section 1, Lines 1 – 4; section 3.1, Lines 5 – 7). This advantage is desirable in the invention disclosed by Cousin as it would have increased the overall throughput of a processor. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to utilize the 34-bit control instructions as disclosed by Simonen with the goal of reducing processor execution time in the invention disclosed by Cousin.

10. Claims 27 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,725,357 (hereinafter Cousin) in view of Andrew S. Tanenbaum; Structured Computer Organization, 1984; Pg. 10 – 11(hereinafter Tanenbaum).

As per claim 27, Cousin teaches the limitations as stated in independent claim 26.

Cousin does not disclose the method of claim 26 being embodied on a computer program product comprising a computer readable medium bearing a program code, which when processed by a computer, causes the computer to be operated according to the method of claim 26.

However, Tanenbaum teaches that "hardware and software are logically equivalent" and that any hardware apparatus can be simulated in software (Tanenbaum; p. 11, Lines 11 – 13). The advantage of implementing the method disclosed within claim 18 within a machine-accessible medium would have been to exploit the advantages of software-based approaches such as cost or ease of upgrading (Tanenbaum; p. 11, Lines 13 – 15). This advantage would have motivated one of ordinary skill in the art to implement the method disclosed in the body of claim 27 in software as opposed to in hardware.

As per claim 28, Cousin teaches the limitations as stated in independent claim 26.

Cousin does not teach the method of claim 26 being embodied in a computer readable medium bearing a program code.

However, Tanenbaum teaches that "hardware and software are logically equivalent" and that any hardware apparatus can be simulated in software (Tanenbaum; p. 11, Lines 11 – 13). The advantage of implementing the method disclosed within claim 18 within a machine-accessible medium would have been to exploit the advantages of software-based approaches such as cost or ease of upgrading (Tanenbaum; p. 11, Lines 13 – 15). This advantage would have motivated one of ordinary skill in the art to implement the method disclosed in the body of claim 28 in software as opposed to in hardware.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to RICHARD FRANKLIN whose telephone number is (571)272-0669. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alford Kindred can be reached on (571) 272-4037. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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